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Clean Version of Amended Specification Paragraphs 2002

Title: MULTI-BANK MEMORY TECHNOLOGY CENTER 2800

Applicant: Brian M. Shirley et al.

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The paragraph beginning on Page 3, line 8 is amended as follows:

Figure 2 shows a prior art sense amplifier suitable for use in a multi-bank memory. Sense amplifier 200 includes N-sense amplifier 202 and P-sense amplifier 204 coupled between sense nodes 232 and 234, isolation transistors 206A, 206B, 208A, and 208B, column decode transistors 210 and 212, and bank select transistors 216 and 218. Sense nodes 232 and 234 are coupled to input output (I/O) lines 224 and 222 through the column decode and bank select transistors. A column decode signal (Y-GATE) on node 214 is coupled to column decode transistors 210 and 212, and a bank select signal (BANK) on node 220 is coupled to bank select transistors 216 and 218. Other column decode lines 230 driven by the column decoder 110 (Figure 1) pass nearby sense amplifier 200. Other column decode lines 230 are coupled to other sense amplifiers (not shown) in the same manner that Y-GATE is coupled to sense amplifier 200 on node 214.

The paragraph beginning on Page 3, line 20 is amended as follows:

The operation of sense amplifier 200 is well known. When data from a memory core either to the left or right of sense amplifier 200 is to be read, the appropriate isolation transistors are turned on by either signal ISOL or ISOR, and the N-sense and P-sense amplifiers are activated using signals NLAT and ACT, respectively. The data value (and its complement) being read appears on sense nodes 232 and 234. When both the column decode signal (Y-GATE) on node 214 and the bank select signal (BANK) on node 220 are asserted, transistors 210, 212, 216, and 218 turn on and couple sense amplifier 200 to I/O lines 222 and 224.

The paragraph beginning on Page 7, line 11 is amended as follows:

Figure 4 shows a sense amplifier in accordance with the present invention. Sense amplifier 400 includes N-sense amplifier 402 and P-sense amplifier 404 coupled between sense nodes 432 and 434, isolation transistors 406A, 406B, 408A, and 408B, and column decode transistors 410 and 412. Sense nodes 432 and 434 are coupled to input output (I/O) lines 424 and 422 through the column decode transistors. A column decode signal (Y-GATE) on node 414 is coupled to column decode transistors 410 and 412.

The paragraph beginning on Page 7, line 24 is amended as follows:

In operation, when data from a memory core either to the left or right of sense amplifier 400 is to be read, the appropriate isolation transistors are turned on by either signal ISOL or ISOR, and the N-sense and P-sense amplifiers are activated using signals NLAT and ACT, respectively. The data value (and its complement) being read appears on sense nodes 432 and 434. When the column decode signal (Y-GATE) on node 414 is asserted, transistors 410 and 412 turn on and couple sense amplifier 400 to I/O lines 422 and 424.